## **CLAIMS**

## What is claimed is:

- 1. A semiconductor device comprising:
  - a dielectric layer;
  - a silicon-nitride layer superjacent to the dielectric layer;
  - a polysilicon gate layer superjacent to the silicon-nitride layer.
- 2. The semiconductor device of claim 1 wherein the silicon-nitride layer has been deposited upon the dielectric layer using a physical vapor deposition (PVD) process.
- 3. The semiconductor device of claim 2 wherein the dielectric layer has a dielectric constant of twenty or greater.
- 4. The semiconductor device of claim 3 wherein the polysilicon gate layer is n-type.
- 5. The semiconductor device of claim 3 wherein the polysilicon gate layer is p-type.
- 6. The semiconductor device of claim 1 wherein the semiconductor device is a complementary metal-oxide-semiconductor device.

- 7. A method comprising:
  forming a dielectric layer upon a semiconductor substrate;
  forming a silicon-nitride layer upon the dielectric layer;
  forming a polysilicon layer upon the silicon-nitride layer.
- 8. The method of claim 7 wherein the silicon-nitride layer is formed by by depositing it upon the dielectric layer using a physical vapor deposition (PVD) process.
- 9. The method of claim 8 wherein the dielectric layer has a dielectric constant of twenty or greater.
- 10. The method of claim 9 wherein the polysilicon gate layer is n-type.
- 11. The method of claim 10 wherein the polysilicon gate layer is p-type.
- 12. The method of claim 8 wherein the dielectric layer, the silicon-nitride layer, and the polysilicon layer are part of a gate structure within a complementary metal-oxide-semiconductor device.
- 13. An apparatus comprising:
  - a gate structure including a silicon-nitride layer;
  - a substrate coupled to the gate structure;

a drain coupled to the substrate; a source coupled to the substrate.

- 14. The apparatus of claim 13 wherein the silicon-nitride layer has been formed by a physical vapor deposition (PVD) process.
- 15. The apparatus of claim 13 wherein the gate structure further includes a dielectric layer coupled to the silicon-nitride layer, the dielectric layer having a dielectric constant greater than twenty.
- 16. The apparatus of claim 13 wherein the gate structure further includes a polysilicon layer coupled to the silicon-nitride layer.
- 17. The apparatus of claim 16 wherein the polysilicon layer comprises n-type material.
- 18. The apparatus of claim 16 wherein the polysilicon layer comprises p-type material.
- 19. The apparatus of claim 13 wherein the gate structure is part of a complementary metal-oxide-semiconductor device.
- 20. A process for forming a semiconductor device comprising:

forming a substrate;

forming a dielectric layer having a dielectric constant greater than twenty upon the substrate;

forming a polysilicon layer, the polysilicon layer being coupled to the dielectric layer by a buffer layer to help prevent electrical shorts between the polysilicon layer and the dielectric layer.

- 21. The process of claim 20 wherein the buffer layer is to help prevent pinning of the polysilicon layer's work function.
- 22. The process of claim 21 wherein the buffer layer is to help reduce defect density between the dielectric layer and the polysilicon layer.
- 23. The process of claim 20 wherein the buffer comprises silicon-nitride.
- 24. The process of claim 23 wherein the silicon nitride is deposited upon the dielectric layer using a physical vapor deposition (PVD) process.
- 25. The process of claim 24 wherein the polysilicon layer, the silicon-nitride layer, and the dielectric layer are part of a gate structure within a complementary metal-oxide-semiconductor (CMOS) device.

26. The process of claim 25 wherein the dielectric layer and the polysilicon layer are formed using CMOS process techniques.